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EXAMINER	
CHANG, SUNRAY	
ART UNIT	**PAPER NUMBER**
2128	6

DATE MAILED: 01/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/668,109	MEYER, STEVEN J.	
	Examiner	Art Unit	
	Sunray Chang	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 5, 12 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. The term "implicit wired operations" in claims 5, 12 and 20 are vague and indefinite. Because of term "Implicit wired operations" is not defined by the specification, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

3. The term "function procedural operations" in claims 5, 12 and 20 is vague and indefinite. Because of term "function procedural operations" is not defined by the specification, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Interpretation

4. The term "implicit wired operations" in claims 5, 12 and 20 is not clearly recited. Based on "common implicit constructs are logic gates implemented by wire connections", examiner interprets the term "implicit wired operations" to be treated as "wire connections"

5. The term "timing-free procedural operations" in claims 5, 12 and 20 has been recited contained in both function and task statements. It is obvious for one has ordinary skill in the art to treat "timing-free procedural operations" as part of "function procedural operations"

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 21 are rejected under 35 U.S.C. 102(b) as being anticioated by William C. Steinmetz (U.S. Patent No. 5,600,579 and Steinmetz hereinafter).

7. Regarding Independent claim 1, Steinmetz teaches a processor (CPU, Col 1, Line 45) having memory (emulated memory device, Col 1, Line 49) for storing (loading into memory, Col 1, Line 56) a program (instruction, Col 1, Line 48) that is capable of being executed (executes, Col 1, Line 48) by processor program (test script, Col 28,

Line 51) directing (steps, Col 28, Line 41) the operation of processor (compiling, Col 28, Line 58) to: convert (coupled, Col 3, Line 8) the HDL coded electronic circuit model (master model, Col 3, Line 8) to binary object code (object code, Col 28, Line 61); and simulate (simulator, Col 27, Line 46) the electronic circuit (hardware, Col 27, Line 46) by utilizing (retrieve, Col 28, Line 61) said binary object code (object code, Col 28, Line 61).

8. Regarding dependent claim 2, Steinmetz teaches program (test script, Col 28, Line 51) directs (steps, Col 28, Line 41) said processor (computer, Col 27, Line 32) to convert (coupled, Col 3, Line 8) the HDL coded electronic circuit model (master model, Col 3, Line 8) to binary object code (object code, Col 28, Line 61) by directing (steps, Col 28, Line 41) said processor (computer, Col 27, Line 32) to translate (coupled, Col 3, Line 8) the HDL coded electronic circuit model (master model, Col 3, Line 8) into an intermediate program language code (master model computer program, Col 28, Line 58) and to compile (compiling, Col 28, Line 58) said intermediate program language code (master model computer program, Col 28, Line 58) to said binary object code (object code, Col 28, Line 61).

9. Regarding dependent claims 3, 10 and 18, Steinmetz teaches intermediate program language code (master model computer program by means of PLI, Col 12, Line 17) is a C program language code (C programming language, Col 2, Line 24).

10. Regarding dependent claims 4, 11 and 19, Steinmetz teaches C program language code (PLI program, 2, 24) is grouped into code types selected from a group consisting of: evaluation C code (functionally, Col 1, Line 46) and scheduling C code (correctly timed, Col 1, Line 46).

11. Regarding dependent claims 5, 12 and 20, Steinmetz teaches binary object code (object code, Col 28, Line 61) performs operations that are selected from a group consisting of: initial/always block operations (block diagram, Fig. 1, 3), timing-free procedural operations (reading data from memory, Col 2, Line 11), task procedural operations (multitasking operating, Col 5, Line 16), function procedural operations reading data from memory, Col 2, Line 11), event control operations (event handling, Col 19, Line 34), delay control operations (set simulation timing, Col 22, Line 25), scheduled procedural operations (set simulation timing, Col 22, Line 25), declarative gate operations (get level model, Col 1, Line 44), continuous assignment operations (get level model, Col 1, Line 44), user-defined primitive operations (defined by user, Col 6, Line 27), implicit wired operations (manipulate wire, Col 22, Line 23), delay path operations (manipulate wire, Col 22, Line 23), system task operations (multitasking operation, Col 5, Line 16), and system service operations (operating system, Col 3, Line 23).

Dependent claims 5, 12 and 20 are drawing to operations such as "block operation", "procedural operation", "event control", "task operation", etc those are inherent in hardware simulators. Examples disclosed by Steinmetz showed above.

12. Regarding dependent claims 6 and 13, Steinmetz teaches program (test script, Col 28, Line 51) directs (steps, Col 28, Line 41) said processor (computer, Col 27, Line 32) to simulate (simulator, Col 27, Line 46) the electronic circuit (hardware, Col 27, Line 46) by utilizing (retrieve, Col 28, Line 61) said object code (object code, Col 28, Line 61) to make calls (corresponding, Col 4, Line 6) to a programming language interface (PLI)(test script computer program, Col 4, Line 8).

13. Regarding dependent claims 7, 14 and 21, "binary object code is utilizable by substantially all types of simulators." Is inherent. For example Steinmetz teaches binary object code (object code, Col 4, Line 11) is utilizable by substantially all types of simulators (verification system, Col 4, Line 12).

14. Regarding independent claim 8, Steinmetz teaches reading (reading, Col 2, Line 11) the HDL coded electronic circuit model (master model, Col 2, Line 5); converting (coupled, Col 3, Line 8) the HDL coded electronic circuit model (master model, Col 3, Line 8) into a linkable simulation program (object code, Col 28, Line 61); and simulating (simulator, Col 27, Line 46) the operation of the electronic circuit (hardware, Col 27, Line 46) by utilizing (retrieve, Col 28, Line 61) said linkable simulation program (object code, Col 28, Line 61).

15. Regarding dependent claims 9 and 17, Steinmetz teaches the steps of translating (coupled, Col 3, Line 8) the HDL coded electronic circuit model (master model, Col 3, Line 8) into an intermediate program language code (master model computer program, Col 28, Line 58) and compiling (compiling, Col 28, Line 58) the intermediate program language code (master model computer program, Col 28, Line 58) to said linkable simulation program (object code, Col 28, Line 61).

16. Regarding independent claim 15, Steinmetz teaches processing means for executing (executes, Col 1, Line 48) a program (instruction, Col 1, Line 48), wherein said program includes a conversion means for converting (coupled, Col 3, Line 8) the HDL coded electronic circuit model (master model, Col 3, Line 8) into a simulator-operable program (object code, Col 28, Line 61) and a simulation means for simulating (simulator, Col 27, Line 46) the HDL coded circuit model (hardware, Col 27, Line 46) by utilizing (retrieve, Col 28, Line 61) said simulator operable program (object code, Col 28, Line 61) to make calls (corresponding, Col 4, Line 6) to a programming language interface (PLI) (test script computer program, Col 4, Line 8).

17. Regarding dependent claim 16, Steinmetz teaches simulator (verification system, Col 28, Line 55) -operable (functions, Col 28, Line 56) program comprises binary object code (object code, Col 28, Line 54).

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Furuichi (U.S. Patent No. 5,437,037) discloses Verilog-HDL, C-language, schedule control, compiled, initial/always function, in-module variable. Stapleton (U.S. Patent No. 5,870,585) discloses RTL, HDL, multi-tasking, memory system, instruction caching, C++, object code, converted. Rompaey et al. (U.S. Patent No. 5,870,588) discloses model, system, simulate, executed on a programmable processor, VHDL, assembly, coding, C, compiler, stored. Pickup et al. (U.S. Patent No. 5,774,380) discloses Verilog, PLI, simulation, sequential. Sano et al. (U.S. Patent No. 5,758,123) discloses assembly, HDL, simulation program, Verilog-XL, Verilog-HDL, compile, assembler language, sequential, scheduler, C-compile, stored.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sunray Chang whose telephone number is 703-305-8744. The examiner can normally be reached on M-F 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-3506.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-6833.

Sunray Chang
Patent Examiner
Group Art Unit 2128
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U.S. Patent and Trademark Office

January 8, 2004

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
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